forming a first trench into a semiconductor substrate;

forming a single layer dielectric lining on the surface of said first trench;

forming a spacer along the sidewall of said first trench over and in direct contact with said single layer dielectric lining;

forming a second trench into said semiconductor substrate at the bottom of said first trench by using said spacer as an etching guide, said semiconductor substrate being devoid of a bordering diffusion region at the base of said second trench;

forming an insulative material in said first and second trenches at least partially by substantially consuming said spacer and said single layer dielectric lining to substantially fill said first and second trenches with said insulative material.

26. (Amended) The process as recited in claim 25, wherein an overall depth of said first and second trenches is two times a depth of a bordering diffusion region.

30. (Twice Amended) The process as recited in claim 25, wherein said step of forming said insulative material comprises:

annealing said semiconductor assembly in the presence of an oxidizing agent.

34. (Three Times Amended) A process for forming device isolation for a semiconductor assembly, said process comprising the steps of:

forming a first trench into a semiconductor substrate;

forming a single layer dielectric lining on the surface of said first trench;

forming a semiconductive spacer along the sidewall of said first trench over and in direct contact with said single layer dielectric lining;

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forming a second trench into said semiconductor substrate at the bottom of said first trench by using said semiconductive spacer as an etching guide, said semiconductor substrate being devoid of a bordering diffusion region at the base of said second trench;

forming an insulative material in said first and second trenches at least partially by substantially consuming said semiconductive spacer and said single layer dielectric lining during formation to substantially fill said first and second trenches with said insulative material;

planarizing said insulative material;

wherein said process uses only one mask to form said device isolation.

D5 amend

35. (Amended) The process as recited in claim 34, wherein an overall depth of said first and second trenches is two times a depth of a bordering diffusion region.

amend D6

37. (Twice Amended) The process as recited in claim 34, wherein said step of forming said insulative material comprises:

annealing said semiconductor assembly in the presence of an oxidizing agent.

38. (Twice Amended) The process as recited in claim 34, wherein said insulative material and said single layer dielectric lining are the same type material.

40. (Three Times Amended) A process for fabricating a semiconductor assembly having device isolation, said process comprising the steps of:

forming a mask over a silicon substrate assembly;

forming a first trench into said silicon substrate assembly using said mask as an etching guide;

forming an oxide layer on the surface of said first trench;

forming a silicon spacer on the sidewall of said first trench over and in direct contact with said single layer dielectric lining;

forming a second trench into said silicon substrate assembly at the bottom of said first trench by using said silicon spacer as an etching guide, said silicon substrate assembly being devoid of a bordering diffusion region at the base of said second trench;

forming an oxide filler in said first and second trenches at least partially by substantially consuming said silicon spacer and said oxide layer to substantially fill said first and second trenches with said oxide filler;

planarizing said oxide filler.

41. (Amended) The process as recited in claim 40, wherein an overall depth of said first and second trenches is two times a depth of a bordering diffusion region.

50. (Three Times Amended) A process for forming device isolation for a semiconductor assembly, said process comprising the steps of:

forming a trench into a semiconductor substrate, said semiconductor substrate being devoid of a bordering diffusion region at the base of said trench;

forming a single layer dielectric lining on the surface of said trench;

forming a semiconductive spacer along the sidewall of said trench over and in direct contact with said single layer dielectric lining;

forming an insulative material in said trench at least partially by substantially consuming said semiconductive spacer and said single layer dielectric lining to substantially fill said trench with said insulative material.

51. (Amended) The process as recited in claim 50, wherein an overall depth of said trench is two times a depth of a bordering diffusion region.

53. (Twice Amended) The process as recited in claim 50, wherein said step of forming an insulative material comprises:

annealing said semiconductor assembly in the presence of an oxidizing agent.

54. (Twice Amended) The process as recited in claim 50, wherein said insulative material and said dielectric lining are the same type material.